AMENDMENTS TO THE CLAIMS

Please amend the claims to read as follows. This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (*Canceled*)

2. (*Currently Amended*) A method for aligning data flows in time division frames, comprising the steps of:

measuring the phase of said input data flow with respect to the phase of a reference signal, for controlling the delay time introduced by a delay line in said input data flow depending on the measured phase, wherein the phase of the input data flow is measured in a time interval approximately corresponding to the transit time of a predefined data sequence comprised in said input data flow,

detecting the flow of said predefined data sequence containing a logic transition ~~is detected~~, and

generating an enable signal activating a phase sampling operation.

3. (*Previously Presented*) The method for aligning data flows in time division frames according to claim 20, wherein, by said enable signal, a masked reference signal is obtained from

the reference signal, said masked reference signal being active only during the passage of the predefined data sequence containing a logic transition.

4. (*Previously Presented*) A method according to claim 20, said method further comprising the step of providing a further delay line with a fixed delay for producing a plurality of delayed phases from the input data flow.

5. (*Previously Presented*) The method for aligning data flows in time division frames according to claim 4, wherein said masked reference signal is used for controlling execution of the sampling operation of said plurality of delayed phases.

6. (*Previously Presented*) The method for aligning data flows in time division frames according to claim 5, wherein a second enable signal is obtained indicating the presence of a logic transition in the predefined data sequence, and said second enable signal is used for activating the sampling operation of said plurality of delayed phases.

7. (*Previously Presented*) The method for aligning data flows in time division frames according to claim 6, wherein said second enable signal is obtained from a correction signal deriving from an alignment operation of the input data flow.

8. (*Previously Presented*) The method for aligning data flows in time division frames according to claim 20, wherein the result of said phase measurement operation is supplied to a control logic, which generates selection signals for controlling the delay time of the delay line, depending on the said result of the phase measurement operation.

9. (*Previously Presented*) The method for aligning data flows in time division frames according to claim 8, wherein the control logic decides whether to increment or decrement by one an index i of the selection signals, provided at least one of the first two delayed phases or one of the last two delayed phases in at least one of a plurality of values sampled during the transit of the predefined sequence, differs from the phase of an aligned data flow.

10. (*Currently Amended*) A method for aligning data flows in time division frames, ~~that provides for~~comprising the steps of measuring the phase of said input data flow with respect to the phase of a reference signal, ~~for~~and controlling the delay time introduced by a delay line in said input data flow depending on the measured phase, wherein

said measuring step comprises measuring the phase of the input data flow ~~is measured~~ in a time interval approximately corresponding to the transit time of a predefined data sequence containing a logic transition, said predefined data sequence being comprised in said input data flow, wherein said predefined data sequence is a frame alignment word and

said time division frames forming the input data flow are either SDH or Sonet frames.

11. (*Canceled*)

12. (*Previously Presented*) A phase alignment circuit of an input data flow in a time division frame, comprising a phase equalizer for equalizing the phase of a reference signal with the phase of the input data flow and driving, through appropriate selection signals, a variable delay line operating on the input data flow, wherein a detector is provided for the transit of a predefined data sequence containing a logic transition comprised in the input data flow, wherein said detector controls the operation of the phase equalizer through an enable signal.

13. (*Previously Presented*) The phase alignment circuit according to claim 21, wherein a logic masker is provided for obtaining a masked clock signal from the combination of the enable signal and reference signal.

14. (*Previously Presented*) A phase alignment circuit according to claim 13, further comprising, downstream of said delay line, a further delay line pertaining to the phase equalizer, which produces a plurality of delayed phases from the input data flow.

15. (*Previously Presented*) The phase alignment circuit of an input data flow in a time division frame according to claim 14, wherein the time delay circuit comprises a sampler of said plurality of delayed phases, which employs the masked clock signal as a clock signal.

16. (*Previously Presented*) The phase alignment circuit of an input data flow in a time division frame according to claim 15, wherein said sampler receives an enable signal generated by the detector, which indicates the transit of the transition in the predefined data sequence.

17. (*Previously Presented*) The phase alignment circuit of an input data flow in a time division frame according to claim 15, wherein the time delay circuit comprises a control logic for receiving the sampled values of the plurality of delayed phases and emitting the selection signals depending on them.

18. (*Currently Amended*) The phase alignment circuit of an input data flow in a time division frame according to claim ~~11~~12, wherein the variable delay line is obtained through a ladder of delay elements.

19. (*Canceled*)

20. (*Previously Presented*) A method for aligning a data flow in time division frames, comprising the steps of:

detecting a pre-defined data sequence contained in said data flow;

in response to detection of said pre-defined data sequence, generating an enable signal during a time interval approximately corresponding to a transit time of said pre-defined data sequence;

in response to said enable signal, activating a measurement of the phase of said data flow with respect to the phase of a reference clock signal in said time interval, wherein the frequency of said reference clock signal is equal to a nominal frequency of said data flow; and

controlling a delay time introduced by a delay line in said data flow depending on the measured phase.

21. (*Previously Presented*) A phase alignment circuit of an input data flow in a time division frame, comprising:

a detector for detecting a pre-defined data sequence contained in said data flow and in response thereto generating an enable signal during a time interval approximately corresponding to a transit time of said pre-defined data sequence;

a phase measurement circuit responsive to said enable signal to measure the phase of said data flow relative to the phase of a reference clock signal in said time interval, wherein the frequency of said reference clock signal is equal lot the nominal frequency of said data flow; and

a time delay circuit for controlling a time delay introduced by a delay line in said data flow depending on the measure phase.